

CLAIMS

1. A circuit for decoding video data, said circuit comprising:

an instruction memory for storing a plurality of executable instructions;

a processor for executing the plurality of executable instructions, the execution of the plurality of executable instructions causing:

storing a portion of a first frame in a row of memory; and

storing a portion of a second frame in the row of memory.

2. The circuit of claim 1, wherein the portion of the first frame and the portion of the second frame comprises a macroblock.

3. The circuit of claim 1, wherein the portion of the first frame is in a top half of the first frame, and wherein the portion of the second frame is in a top half of the second frame.

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4. A circuit for decoding video data, said circuit comprising:

an instruction memory for storing a plurality of executable instructions;

a processor for executing the plurality of executable instructions, the execution of the plurality of executable instructions causing:

storing a first macroblock row of a first frame in a first one or more rows of memory;

storing a first macroblock row of a second frame in a second one or more rows of memory; and

a particular one of the first one or more rows of memory being adjacent to a particular one of the second one or more rows of memory.

5. The circuit of claim 4, wherein the first one or more rows of memory are contiguous, and wherein the second one or more rows of memory are contiguous.

6. The circuit of claim 4, wherein execution of the plurality of instructions further causes:

storing a first macroblock row of a third frame in a third one or more rows of memory; and

wherein a particular one of the third one or more rows of memory are adjacent to another particular one of the second one or more rows of memory.

7. The circuit of claim 6, wherein execution of the plurality of instructions further causes:

storing a second macroblock row of the first frame in a fourth one or more rows of memory;

the third one or more rows of memory being continuous;  
and

wherein a particular one of the fourth one or more rows is adjacent to another particular one of the third one or more rows of memory.

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8. A method for decoding video data, said method comprising:

storing a portion of a first frame in a row of memory;  
and

storing a portion of a second frame in the row of memory.

9. The method of claim 8, wherein the portion of the first frame and the portion of the second frame comprises a macroblock.

10. The method of claim 8, wherein the portion of the first frame is in a top half of the first frame, and wherein the portion of the second frame is in a top half of the second frame.

11. A method for decoding video data, said method comprising:

storing a first macroblock row of a first frame in a first one or more rows of memory;

storing a first macroblock row of a second frame in a second one or more rows of memory; and

a particular one of the first one or more rows of memory being adjacent to a particular one of the second one or more rows of memory.

12. The method of claim 11, wherein the first one or more rows of memory are contiguous, and wherein the second one or more rows of memory are contiguous.

13. The method of claim 12, wherein execution of the plurality of instructions further causes:

storing a first macroblock row of a third frame in a third one or more rows of memory; and

wherein a particular one of the third one or more rows of memory are adjacent to another particular one of the second one or more rows of memory.

14. The method of claim 13, further comprising:

storing a second macroblock row of the first frame in a fourth one or more rows of memory;

the third one or more rows of memory being continuous; and

wherein a particular one of the fourth one or more rows is adjacent to another particular one of the third one or more rows of memory.